WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

a programmable storage location storing a first temperature limit value, the programmable storage location accessible via an instruction executed by the integrated circuit; and

compare logic coupled to the temperature sensor and the storage location to provide an indication of a comparison between the temperature measurement and the first temperature limit value.

2. The integrated circuit as recited in claim 1 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value.

3. The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement indicated by the temperature sensor falls below a programmable second temperature limit value.

4. The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, in response to access to a control location in the integrated circuit.

5. The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement falls below a programmable second temperature limit value or when a control location in the integrated circuit is accessed, according to a programmable mode of operation.

6. The integrated circuit as recited in claim 2 wherein the first temperature limit value is a panic value indicating a temperature limit for safe integrated circuit operation.

Sub D1

7. The integrated circuit as recited in claim 1 further comprising an addressable storage location coupled to the temperature sensor, the addressable storage location accessible by an instruction executed the integrated circuit and supplying an indication of the temperature measurement on the integrated circuit.

Sub B1

8. The integrated circuit as recited in claim 1 further comprising:
a second output terminal coupled to provide external to the integrated circuit an asserted signal when the temperature measurement indicated by the temperature sensor is above a second temperature limit value.

Sub D1

9. The integrated circuit as recited in claim 8 further comprising:
a second storage location supplying the second temperature limit value; and
second compare logic coupled to the second storage location and coupled to receive the temperature measurement of the integrated circuit, and
wherein the second compare logic generates a second indication of when the temperature measurement of the integrated circuit is above the second temperature limit value.

10. The integrated circuit as recited in claim 9 further comprising:
a third storage location supplying a third temperature limit value;
third compare logic coupled to the third storage location and coupled to receive the temperature measurement, and wherein the compare logic generates a third indication that the temperature measurement of the integrated circuit is below the third temperature limit value.

11. The integrated circuit as recited in claim 1 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement indicated by the temperature sensor is below the third temperature limit value.

12. The integrated circuit as recited in claim 1 wherein the integrated circuit is a microprocessor.

13. A method comprising:
measuring a temperature of an integrated circuit with a temperature sensor, the temperature sensor being a circuit within the integrated circuit;
comparing the measured temperature to a first limit value stored in the integrated circuit; and
generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit.

14. The method as recited in claim 13 wherein the signal is asserted when the measured temperature is less than the first limit value.

15. The method as recited in claim 14 wherein the asserted signal is used to inhibit a cooling device to control the temperature of the integrated circuit.

16. The method as recited in claim 13 wherein the signal is asserted when the measured temperature is greater than the first limit value.

17. The method as recited in claim 16 wherein the signal on the first output terminal is deasserted when a control location on the integrated circuit is accessed or when the measured temperature goes below a lower limit value, according to a programmable mode of operation.

18. The method as recited in claim 16 wherein the signal is utilized to directly control a cooling device.

19. The method as recited in claim 16 further comprising:
comparing the measured temperature to a lower limit value; and
deasserting the signal when the measured temperature is below the lower limit value.

Sub B4

20. The method as recited in claim 16 further comprising accessing a control location in the integrated circuit to cause the signal to be deasserted.

21. The method as recited in claim 16 wherein the asserted signal causes assertion of an interrupt and wherein a sequence of instructions, responsive to the asserted interrupt, activates a cooling device.

Sub D1

22. The method as recited in claim 21 wherein an instruction sequence causes the signal to be deasserted.

Sub B5

23. The method as recited in claim 13 further comprising:
comparing the measured temperature to a second limit value stored in the integrated circuit; and
asserting a second signal on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby indicating that temperature has exceeded a safe limit.

24. The method as recited in claim 23 wherein the second signal is deasserted by accessing a control location in the integrated circuit.

Sub D1

25. An apparatus comprising:
a processor including,
means for measuring temperature of the processor and providing a measured temperature;
means for comparing the measured temperature to at least two limit values; and
two output terminals on the processor coupled to supply an indication of results the comparison.

26. The apparatus as recited in claim 25 wherein the apparatus is a computer system and further comprises at least one cooling device, which activates in response to an asserted signal on at least one of the two output terminals.

27. A microprocessor comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

at least a first and second temperature limit value stored in programmable storage locations in the microprocessor, the storage locations being accessible via software executed by the microprocessor;

compare logic coupled to the temperature sensor and to the programmable storage locations storing the first and second temperature limit values, to provide respectively a first and second signal indicative of a comparison between the temperature measurement and the first and second temperature limit values; and

first and second output terminals coupled to provide respectively, the first and second signals.

28. The microprocessor as recited in claim 27 wherein the microprocessor deasserts the first signal, which is supplied on the first output terminal of processor, when the temperature measurement falls below a programmable third temperature limit value, thereby providing a thermostat mode of operation for the first signal.

29. The integrated circuit as recited in claim 27 wherein the microprocessor includes a software accessible control register controlling operation of the compare logic and the first and second output terminals.